

## CLAIMS

What is claimed is:

- 1 1. A method comprising:  
2 aligning first and second sets of terminals of an integrated circuit (IC) with  
3 corresponding third and fourth sets of terminals of a substrate, the first and second  
4 sets of terminals being in first and second zones, respectively, of the IC;  
5 coupling the first and third sets of terminals with a first type of connector;  
6 and  
7 coupling the second and fourth sets of terminals with a second type of  
8 connector.
- 1 2. The method recited in claim 1, including forming the first and second sets of  
2 terminals on a surface of the IC.
- 1 3. The method recited in claim 2, including forming the first zone in a central  
2 region of the surface.
- 1 4. The method recited in claim 2, including forming the second zone in a  
2 peripheral region of the surface.
- 1 5. The method recited in claim 1, wherein coupling the first and third sets of  
2 terminals with the first type of connector comprises using solder.
- 1 6. The method recited in claim 1, wherein coupling the second and fourth sets  
2 of terminals with the second type of connector comprises using a solderless,  
3 compliant, electrically conductive material.

1 7. The method recited in claim 1, wherein coupling the second and fourth sets  
2 of terminals with the second type of connector comprises using a connector from the  
3 group comprising a nanospring, a sea of leads connector, and an interposer.

1 8. The method recited in claim 1, wherein coupling the second and fourth sets  
2 of terminals with the second type of connector comprises physically compressing  
3 the IC and the substrate together.

1 9. A method comprising:  
2 aligning first and second sets of terminals of an integrated circuit (IC)  
3 package with corresponding third and fourth sets of terminals of a substrate, the first  
4 and second sets of terminals being in first and second zones, respectively, of the IC  
5 package;  
6 coupling the first and third sets of terminals with a first type of connector;  
7 and  
8 coupling the second and fourth sets of terminals with a second type of connector.

1 10. The method recited in claim 9, including forming the first and second sets of  
2 terminals on a surface of the IC package.

1 11. The method recited in claim 10, including forming the first zone in a central  
2 region of the surface.

1 12. The method recited in claim 10, including forming the second zone in a  
2 peripheral region of the surface.

1 13. The method recited in claim 9, wherein coupling the first and third sets of  
2 terminals with the first type of connector comprises using solder.

1 14. The method recited in claim 9, wherein coupling the second and fourth sets  
2 of terminals with the second type of connector comprises using a solderless,  
3 compliant, electrically conductive material.

1 15. The method recited in claim 9, wherein coupling the second and fourth sets  
2 of terminals with the second type of connector comprises using a connector from the  
3 group comprising a nanospring, a sea of leads connector, and an interposer.

1 16. The method recited in claim 9, wherein coupling the second and fourth sets  
2 of terminals with the second type of connector comprises physically compressing  
3 the IC package and the substrate together.

1 17. An electronic package comprising:  
2 a die comprising first and second sets of terminals disposed in first and  
3 second zones, respectively, of the die;  
4 a substrate comprising third and fourth sets of terminals;  
5 a first type of connector to couple the first and third sets of terminals; and  
6 a second type of connector to couple the second and fourth sets of terminals.

1 18. The electronic package recited in claim 17, wherein the first and second sets  
2 of terminals are disposed on a surface of the die.

1 19. The electronic package recited in claim 17, wherein the first zone is centrally  
2 located on the surface.

1 20. The electronic package recited in claim 17, wherein the second zone is  
2 peripherally located on the surface.

1 21. The electronic package recited in claim 17, wherein the first type of  
2 connector comprises solder.

1 22. The electronic package recited in claim 17, wherein the second type of  
2 connector comprises a compliant, electrically conductive material.

1 23. The electronic package recited in claim 17, wherein the second type of  
2 connector is from the group comprising a nanospring, a sea of leads connector, and  
3 an interposer.

1 24. The electronic package recited in claim 17, wherein the second type of  
2 connector comprises an interposer, and wherein the electronic package further  
3 comprises:  
4 an element to physically compress the die and the substrate together to  
5 electrically couple the die to the substrate.

1 25. The electronic package recited in claim 24, wherein the interposer  
2 comprises:  
3 a flexible support formed of electrically insulating material; and  
4 a plurality of elements formed of electrically conductive material.

1 26. The electronic package recited in claim 17, wherein the second type of  
2 connector comprises a compressible element to electrically couple the die to the  
3 substrate.

1 27. The electronic package recited in claim 17, wherein the die further  
2 comprises a fifth set of terminals disposed in a third zone of the die, wherein the  
3 substrate comprises a sixth set of terminals, and wherein the electronic package  
4 further comprises:  
5 a third type of connector to couple the fifth and sixth sets of terminals.



1 34. The electronic assembly recited in claim 31, wherein the second type of  
2 connector is from the group comprising a nanospring, a sea of leads connector, and  
3 an interposer.

1 35. The electronic assembly recited in claim 31, wherein the second type of  
2 connector comprises an interposer, and wherein the electronic assembly further  
3 comprises:  
4 an element to physically compress the IC package and the substrate together  
5 to electrically couple the IC package to the substrate.

1 36. An electronic system having at least one electronic assembly comprising:  
2 a die comprising first and second sets of terminals disposed in first and  
3 second zones, respectively, of a surface of the die;  
4 a substrate comprising third and fourth sets of terminals;  
5 a first type of connector to couple the first and third sets of terminals; and  
6 a second type of connector to couple the second and fourth sets of terminals.

1 37. The electronic system recited in claim 36, wherein the first zone is centrally  
2 located on the surface, and wherein the first type of connector comprises solder.

1 38. The electronic system recited in claim 36, wherein the second zone is  
2 peripherally located on the surface, and wherein the second type of connector  
3 comprises a compliant, electrically conductive material.

1 39. A data processing system comprising:  
2 a bus coupling components in the data processing system; and  
3 a processor coupled to the bus and including at least one electronic package  
4 comprising:

5 a die comprising first and second sets of terminals disposed in first and  
6 second zones, respectively, of a surface of the die;  
7 a substrate comprising third and fourth sets of terminals;  
8 a first type of connector to couple the first and third sets of terminals; and  
9 a second type of connector to couple the second and fourth sets of terminals.

1 40. The data processing system recited in claim 39, wherein the first zone is  
2 centrally located on the surface, and wherein the first type of connector comprises  
3 solder.

1 41. The data processing system recited in claim 39, wherein the second zone is  
2 peripherally located on the surface, and wherein the second type of connector  
3 comprises a compliant, electrically conductive material.

1 42. The data processing system recited in claim 39 and further comprising:  
2 a display coupled to the bus; and  
3 external memory coupled to the bus.